What is claimed is:

1. A hardware description verifying system comprising:

a storage unit which stores a source program for hardware description in a program language;

an output unit; and

a processor which detect a portion of said source program different in logic interpretation between a case of compiling said source program using a compiler and a case of behavioral synthesis, and outputs existence of said source program portion to said output unit.

2. The hardware description verifying system according to claim 1, wherein said processor detects said source program portion in which a variable of a register type is referred to at a clock timing after substitution to said variable at said clock timing.

3. The hardware description verifying system according to claim 2, wherein said processor comprises:

a signal list storage section; and

a processing section which sequentially reads out sentences of said source program, deletes a storage content in said signal list storage section when the read out sentence indicates a clock boundary,

stores said variable in said signal list storage section when said read out sentence indicates the substitution to said variable at said clock timing, and outputs the existence of said read out sentence to said output unit when said read out sentence refers to said variable which is stored in said signal list storage section.

4. The hardware description verifying system according to claim 1, wherein said processor detects said source program portion in which substitution to a variable of a non-overwrite type is carried out twice or more at a clock timing.

5. The hardware description verifying system according to claim 4, wherein said processor comprises:

a signal list storage section; and

a processing section which sequentially reads out sentences of said source program, deletes a storage content in said signal list storage section when the read out sentence indicates a clock boundary, stores said variable in said signal list storage section when said read out sentence indicates the substitution to said variable at said clock timing and said variable is not stored in said signal list storage section, and outputs the existence of said

read out sentence to said output unit when said read out sentence indicates the substitution to said variable at said clock timing and said variable is stored in said signal list storage section.

6. The hardware description verifying system according to claim 1, wherein said processor detects said source program portion in which a variable for a non-register type is referred to at a clock timing without substitution of said value to said variable at said clock timing.

7. The hardware description verifying system according to claim 6, wherein said processor comprises:

a signal list storage section; and

a processing section which sequentially reads out sentences of said source program, deletes a storage content in said signal list storage section when the read out sentence indicates a clock boundary, stores said variable in said signal list storage section when said read out sentence indicates the substitution to said variable at said clock timing, and outputs the existence of said read out sentence to said output unit when said read out sentence refers to said variable which is not stored in said signal list storage section, at said clock timing.

8. The hardware description verifying system according to claim 1, wherein said processor detects said source program portion in which a variable of a wiring line is referred to at a clock timing and then a value is substituted to said variable at said clock timing.

9. The hardware description verifying system according to claim 8, wherein said processor comprises:

a signal list storage section; and

a processing section which sequentially reads out sentences of said source program, deletes a storage content in said signal list storage section when the read out sentence indicates a clock boundary, stores said variable in said signal list storage section when said read out sentence indicates the substitution to said variable at said clock timing, and outputs the existence of said read out sentence to said output unit when said read out sentence refers to said variable which is not stored in said signal list storage section, at said clock timing.

10. The hardware description verifying system according to claim 1, wherein said processor detects said source program portion in which a logical operator is used and a right operand of the operator

type includes a variable with substitution.

11. A hardware description verifying method comprising:

(a) detecting a portion of a source program different in logic interpretation between a case of compiling said source program using a compiler and a case of behavioral synthesis, said source program for hardware description being described in a program language; and

(b) alarming existence of said source program portion.

12. The hardware description verifying method according to claim 11, wherein said source program portion is a portion in which a variable of a register type is referred to a clock timing after substitution to said variable at said clock timing.

13. The hardware description verifying method according to claim 12, wherein said (a) detecting comprises:

sequentially reading out sentences of said source program;

deleting a storage content in a signal list storage section when the read out sentence indicates a clock boundary;

storing said variable in said signal list storage section when said read out sentence indicates the substitution to said variable at said clock timing; and

detecting said read out sentence as said source program portion when said read out sentence refers to said variable which is stored in said signal list storage section.

14. The hardware description verifying method according to claim 11, wherein said source program portion is a portion in which substitution to a variable of a non-overwrite type is carried out twice or more at a clock timing.

15. The hardware description verifying method according to claim 14, wherein said (a) detecting comprises:

sequentially reading out sentences of said source program;

deleting a storage content in a signal list storage section when the read out sentence indicates a clock boundary;

storing said variable in said signal list storage section when said read out sentence indicates the substitution to said variable at said clock timing and said variable is not stored in said signal list

storage section; and

detecting said source program portion when said read out sentence indicates the substitution to said variable at said clock timing and said variable is stored in said signal list storage section.

16. The hardware description verifying method according to claim 11, wherein said source program portion is a portion in which a variable for a non-register type is referred to at a clock timing without substitution of said value to said variable at said clock timing.

17. The hardware description verifying method according to claim 16, wherein said (a) detecting comprises:

sequentially reading out sentences of said source program;

deleting a storage content in a signal list storage section when the read out sentence indicates a clock boundary;

storing said variable in said signal list storage section when said read out sentence indicates the substitution to said variable at said clock timing; and

detecting said source program portion when said read out sentence refers to said variable which

is not stored in said signal list storage section, at said clock timing.

18. The hardware description verifying method according to claim 11, wherein said source program portion is a portion in which a variable of a wiring line is referred to at a clock timing and then a value is substituted to said variable at said clock timing.

19. The hardware description verifying method according to claim 18, wherein said (a) detecting comprises:

sequentially reading out sentences of said source program;

deleting a storage content in said signal list storage section when the read out sentence indicates a clock boundary;

storing said variable in said signal list storage section when said read out sentence indicates the substitution to said variable at said clock timing; and

detecting said source program portion when said read out sentence refers to said variable which is not stored in said signal list storage section, at said clock timing.

20. The hardware description verifying method

according to claim 11, wherein said processor detects said source program portion in which a logical operator is used and a right operand of the operator type includes a variable with substitution.

21. A program for a hardware description verifying method comprising:

(a) detecting a portion of a source program different in logic interpretation between a case of compiling said source program using a compiler and a case of behavioral synthesis, said source program for hardware description being described in a program language; and

(b) alarming existence of said source program portion.

22. The program according to claim 21, wherein said source program portion is a portion in which a variable of a register type is referred to at a clock timing after substitution to said variable at said clock timing.

23. The program according to claim 22, wherein said (a) detecting comprises:

sequentially reading out sentences of said source program;

deleting a storage content in a signal list

storage section when the read out sentence indicates a clock boundary;

storing said variable in said signal list storage section when said read out sentence indicates the substitution to said variable at said clock timing; and

detecting said read out sentence as said source program portion when said read out sentence refers to said variable which is stored in said signal list storage section.

24. The program according to claim 21, wherein said source program portion is a portion in which substitution to a variable of a non-overwrite type is carried out twice or more at a clock timing.

25. The program according to claim 24, wherein said (a) detecting comprises:

sequentially reading out sentences of said source program;

deleting a storage content in a signal list storage section when the read out sentence indicates a clock boundary;

storing said variable in said signal list storage section when said read out sentence indicates the substitution to said variable at said clock timing and said variable is not stored in said signal list

storage section; and

detecting said source program portion when said read out sentence indicates the substitution to said variable at said clock timing and said variable is stored in said signal list storage section.

26. The program according to claim 21, wherein said source program portion is a portion in which a variable for a non-register type is referred to at a clock timing without substitution of said value to said variable at said clock timing.

27. The program according to claim 26, wherein said (a) detecting comprises:

sequentially reading out sentences of said source program;

deleting a storage content in a signal list storage section when the read out sentence indicates a clock boundary;

storing said variable in said signal list storage section when said read out sentence indicates the substitution to said variable at said clock timing; and

detecting said source program portion when said read out sentence refers to said variable which is not stored in said signal list storage section, at said clock timing.

28. The program according to claim 21, wherein said source program portion is a portion in which a variable of a wiring line is referred to at a clock timing and then a value is substituted to said variable at said clock timing.

29. The program according to claim 28, wherein said (a) detecting comprises:

sequentially reading out sentences of said source program;

deleting a storage content in said signal list storage section when the read out sentence indicates a clock boundary;

storing said variable in said signal list storage section when said read out sentence indicates the substitution to said variable at said clock timing; and

detecting said source program portion when said read out sentence refers to said variable which is not stored in said signal list storage section, at said clock timing.

30. The program according to claim 21, wherein said processor detects said source program portion in which a logical operator is used and a right operand of the operator type includes a variable with substitution.